

REMARKS

Applicants respectfully request further examination and reconsideration in view of the following remarks. Claims 15-30 remain pending in the case. Claims 15-30 are rejected. Claims 16, 18, 29 and 30 are amended herein. No new matter has been added.

35 U.S.C. §103(a)

Claims 16-18, 20-26, 29 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 5,739,569 by Chen, hereinafter the “Chen” reference, in view of United States Patent 5,879,990 by Dormans, et al., hereinafter the “Dormans” reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 16-18, 20-26, 29 and 30 are not anticipated nor rendered obvious by Chen in view of Dormans.

Independent Claim 16 recites (emphasis added):

A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer;

forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer; and
siliciding said bitlines.

Claims 17, 18, 20-26, 29 and 30 that depend from independent Claim 16 provide further recitations of the limitations of the present invention as claimed.

The combination of Chen and Dormans does not teach a method for fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed. Chen and the claimed embodiments of the claimed invention are very different. Applicants understand Chen to teach a non-volatile memory cell having a floating gate connected to a source and to a ground. As pointed out by the Examiner, Chen does not show siliciding a bitline.

With reference to Figure 2 of Chen, Applicants understand Chen to teach a memory cell having a source 10 and a drain 12. All of the source electrodes 10 are connected to a bit line (BL1 through BL4). In particular, all the drain regions 12 are connected to ground (col. 4, lines 16-18 and lines 30-32). As shown, the drain regions 12 are explicitly not connected to a bit line. Furthermore, by teaching that drain electrode 12 is not connected to a bit line, but rather is connected to ground, Chen teaches away from drain 12 being a bit line.

In contrast, the claimed embodiments recite a method for fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer” (emphasis added). With reference to Figure 6 of the current application, a gate is shown (ONO layer 302 and layer 311) wherein bitlines 324 are formed on both sides of the gate (page 6, lines 10-22).

Moreover, as pointed out by the Examiner, Chen does not teach siliciding a bitline. The combination of Chen and Dormans fails to teach or suggest the claim limitation of “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” because Dormans does not overcome the shortcomings of Chen. Dormans, alone or in combination with Chen, does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed. As described above, Chen teaches a non-volatile memory cell with oxide and nitride tunneling layers and without a bitline.

Applicants understand Dormans to teach a semiconductor device having an embedded non-volatile memory. Dormans does not teach, show or suggest fabricating a memory cell, as claimed. Specifically, Dormans does not teach, describe or suggest a memory cell including a bitline. Applicants respectfully assert that, Dormans does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed.

Furthermore, as described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. In particular, the ground is not a

bitline. In contrast, by teaching that the drain electrode is not connected to a bit line, but rather is connected to ground, Chen teaches away from such a configuration.

In view of the claim limitation of “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer” not being shown or suggested in Dormans, in combination with the above arguments, Applicants respectfully submit that independent Claim 16 overcome the cited references and are therefore allowable over the combination of Chen and Dormans.

Applicants respectfully assert that nowhere does the combination of Chen and Dormans teach, disclose or suggest the present invention as recited in independent Claim 16, that this claim overcomes the Examiner’s basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Chen and Dormans also does not show or suggest the additional claimed features of the present invention as recited in Claims 17, 18, 20-26, 29 and 30 which depend from independent Claim 16. Therefore, Applicants respectfully submit that Claims 15 and 17, 18, 20-26, 29 and 30 overcome the Examiner’s basis for rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Dormans, and further in view of United States Patent 5,942,782 by Hsu,

hereinafter the “Hsu” reference. Claim 15 depends from independent Claim 16.

Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claim 16 is not anticipated nor rendered obvious by Chen in view of Dormans, and further in view of Hsu.

The combination of Chen, Dormans and Hsu fails to teach or suggest the claim limitation of “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” because Hsu does not overcome the shortcomings of the combination of Chen and Dormans. Hsu, alone or in combination with Chen and Dormans, does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed.

As described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. Furthermore, Dormans teaches a semiconductor device having an embedded non-volatile memory that is not connected to a bitline.

Applicants understand Hsu to teach an electrostatic protection component. In particular, Hsu does not teach, describe or suggest a memory cell including bitlines formed on both sides of a gate.

Applicants respectfully assert that nowhere does the combination of Chen, Dormans and Hsu teach, disclose or suggest the present invention as recited in independent Claim 16, that this claim overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Chen, Dormans and Hsu also does not show or suggest the additional claimed features of the present invention as recited in Claim 15 which depends from independent Claim 16. Therefore, Applicants respectfully submit that Claim 15 overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a) as this claim is dependent on an allowable base claim.

Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Dormans, and further in view of United States Patent 6,218,695 by Nachumovsky, hereinafter the "Nachumovsky" reference. Claim 19 depends from independent Claim 16. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claim 16 is not anticipated nor rendered obvious by Chen in view of Dormans, and further in view of Nachumovsky.

The combination of Chen, Dormans and Nachumovsky fails to teach or suggest the claim limitation of "forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer," because Nachumovsky does not

overcome the shortcomings of the combination of Chen and Dormans. Nachumovsky, alone or in combination with Chen and Dormans, does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed.

As described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. Furthermore, Dormans teaches a semiconductor device having an embedded non-volatile memory that is not connected to a bitline. Applicants understand Nachumovsky to teach area efficient column select circuitry. In particular, Nachumovsky is silent as to how the memory cells of the circuitry are fabricated. In particular, Nachumovsky does not teach, describe or suggest a process for fabricating a memory cell including “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer” (emphasis added).

Furthermore, as described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. In particular, the ground is not a bitline. In contrast, by teaching that the drain electrode is not connected to a bit line, but rather is connected to ground, Chen teaches away from such a combination.

Applicants respectfully assert that nowhere does the combination of Chen, Dormans and Nachumovsky teach, disclose or suggest the present invention as recited in

independent Claim 16, that this claim overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Chen, Dormans and Nachumovsky also does not show or suggest the additional claimed features of the present invention as recited in Claim 19 which depends from independent Claim 16. Therefore, Applicants respectfully submit that Claim 19 overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a) as this claim is dependent on an allowable base claim.

Claim 27 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Dormans, and further in view of United States Patent 5,859,454 by Choi et al., hereinafter the "Choi" reference. Claim 27 depends on independent Claim 16. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claim 16 is not anticipated nor rendered obvious by Chen in view of Dormans, and further in view of Choi.

The combination of Chen, Dormans and Choi fails to teach or suggest the claim limitation of "forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer," because Choi does not overcome the shortcomings of the combination of Chen and Dormans. Choi, alone or in combination with Chen and Dormans, does not show or suggest a process of fabricating a memory cell

comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer,” as claimed.

As described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. Furthermore, Dormans teaches a semiconductor device having an embedded non-volatile memory that is not connected to a bitline.

Applicants understand Choi to teach a non-volatile memory device, but is silent as to how the memory device is fabricated. In particular, Choi does not teach, describe or suggest a process for fabricating a memory cell including “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer” (emphasis added).

Furthermore, as described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. In particular, the ground is not a bitline. In contrast, by teaching that the drain electrode is not connected to a bit line, but rather is connected to ground, Chen teaches away from such a combination.

Applicants respectfully assert that nowhere does the combination of Chen, Dormans and Choi teach, disclose or suggest the present invention as recited in independent Claim 16, that this claim overcomes the Examiner’s basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants

respectfully submit that the combination of Chen, Dormans and Choi also does not show or suggest the additional claimed features of the present invention as recited in Claim 27 which depends from independent Claim 16. Therefore, Applicants respectfully submit that Claim 27 overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a) as this claim is dependent on an allowable base claim.

Claim 28 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Dormans, and further in view of United States Patent 6,218,695 by Eitan, hereinafter the "Eitan" reference. Claim 28 depends on independent Claim 16. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claim 16 is not anticipated nor rendered obvious by Chen in view of Dormans, and further in view of Eitan.

The combination of Chen, Dormans and Eitan fails to teach or suggest the claim limitation of "forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer," because Eitan does not overcome the shortcomings of the combination of Chen and Dormans. Eitan, alone or in combination with Chen and Dormans, does not show or suggest a process of fabricating a memory cell comprising "forming bitlines on both sides of said gate subsequent to said forming said gate comprising said polysilicon layer," as claimed.

As described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. Furthermore, Dormans teaches a semiconductor device having an embedded non-volatile memory that is not connected to a bitline.

Applicants understand Eitan to teach a NROM cell with a pocket implant self-aligned to at least one bit line junction. In particular, Eitan teaches a memory cell requiring two functional bit lines for each transistor (col. 1, lines 36-40).

Applicants respectfully submit that grounding a bit line of Eitan would render Eitan inoperable for its intended purpose. In order to optimize the interconnect density in Eitan, two bit lines are used. In contrast, interconnect density is not a concern in Chen. A memory cell designer would not constrain themselves to the limitations of Eitan where there is no need for a second bit line. Therefore, there is no motivation to combine the teachings of Chen with Eitan. In contrast, by teaching a memory cell requiring two functional bit lines, Eitan teaches away from such a combination.

Furthermore, as described above, Chen teaches a non-volatile memory cell having a floating gate connected to a source and to a ground. In particular, the ground is not a bitline. In contrast, by teaching that the drain electrode is not connected to a bit line, but rather is connected to ground, Chen teaches away from such a combination.

Applicants respectfully assert that nowhere does the combination of Chen, Dormans and Eitan teach, disclose or suggest the present invention as recited in independent Claim 16, that this claim overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Chen, Dormans and Eitan also does not show or suggest the additional claimed features of the present invention as recited in Claim 28 which depends from independent Claim 16. Therefore, Applicants respectfully submit that Claim 28 overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a) as this claim is dependent on an allowable base claim.

CONCLUSION

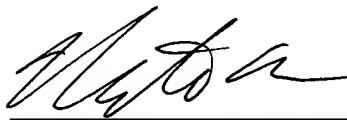
Based on the arguments presented above, Applicants respectfully assert that Claims 15-30 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge our deposit account No. 23-0085 for any unpaid fees.

Respectfully submitted,
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